500 mA Differential Driver & Dual Low Noise (VF) Amplifiers

AD816

FEATURES
Flexible Configuration
- **Two Low Noise Voltage Feedback Amplifiers with High Current Drive, Ideal for ADSL Receivers or Drivers for Low Impedance Loads such as CRT Coils**
- **Two High Current Drive Amplifiers, Ideal for an ADSL Differential Driver or Single Ended Drivers for Low Impedance Loads such as CRT Coils**

Thermal Overload Protection

CURRENT FEEDBACK AMPLIFIERS/DRIVERS
High Output Drive
- **26 dBm Differential Line Drive for ADSL Transmitters**
- **40 V p-p Differential Output Voltage, R_L = 50 Ω @ 1 MHz**
- **500 mA Continuous Current, R_L = 5 Ω**
- **1 A Peak Current, 1% Duty Cycle, R_L = 15 Ω for DMT**

Low Distortion
- **–68 dB @ 1 MHz THD, R_L = 100 Ω, V_O = 40 V p-p**

High Speed
- **120 MHz Bandwidth (–3 dB)**
- **1500 V/µs Differential Slew Rate, V_O = 10 V p-p, G = +5**
- **70 ns Settling Time to 0.1%**

VOLTAGE FEEDBACK AMPLIFIERS/RECEIVERS
High Input Performance
- **4 nV/$\sqrt{Hz}$ Voltage Noise**
- **15 mV Max Input Offset Voltage**

Low Distortion
- **–68 dB @ 1 MHz THD, V_O = 10 V p-p, R_L = 200 Ω**

High Speed
- **100 MHz Bandwidth (–3 dB)**
- **180 V/µs Slew Rate**

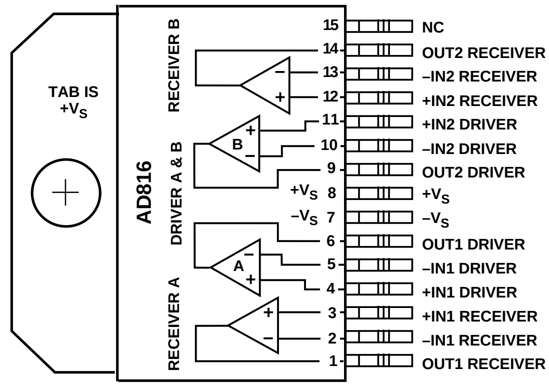
High Output Drive
- **70 mA Output Current Drive**

APPLICATIONS
ADSL, VDSL & HDSL Line Interface Driver & Receiver
CRT Convergence & Astigmatism Adjustment
Coil & Transformer Drivers
Composite Audio Amplifiers

PRODUCT DESCRIPTION

The AD816 consists of two high current drive and two low noise amplifiers. These can be configured differentially for driving low impedance loads and receiving signals over twisted pair cable or could be used independently for single ended driving application such as correction circuits within high resolution CRT Monitors.

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

The two high output drive amplifiers are capable of supplying a minimum of 500 mA continuous output current and up to 1A peak output current, and when configured differentially, 40 V p-p differential output swing can be achieved on ±15 V supplies into a load of 50 Ω. The drivers have 120 MHz of bandwidth and 1,500 V/µs of differential slew rate while featuring total harmonic distortion of –68 dB at 1 MHz into a 100 Ω load, specifications required for high frequency telecommunication subscriber line drivers.

The low noise voltage feedback amplifiers are fully independent and can be configured differentially for use as receiver amplifiers within a subscriber line hybrid interface or individually for signal conditioning or filtering. The low noise of 4 nV/$\sqrt{Hz}$ and distortion of –68 dB at 1 MHz enable low level signals to be resolved and amplified in the presence of large common-mode voltages. 100 MHz of bandwidth and 180 V/µs of slew rate combined with a load drive capability of 70 mA enable these amplifiers to drive passive filters and low inductance coils. The AD816 has thermal overload protection for system reliability and is available in low thermal resistance power packages. The AD816 operates over the industrial temperature range (–40°C to +85°C).

REV. 0

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AD816–SPECIFICATIONS

DRIVER AMPLIFIERS (@ T_A = +25°C, V_S = ±15 V dc, R_F = 1 kΩ and R_{LOAD} = 50 Ω unless otherwise noted)

Model	Conditions	V_S	AD816A Min	AD816A Typ	AD816A Max	Units
DYNAMIC PERFORMANCE						
Small Signal Bandwidth (–3 dB)	G = +2, R_F = 499 Ω, V_{IN} = 0.125 V rms, R_L = 100 Ω	±15	100	120		MHz
	G = +2, R_F = 499 Ω, V_{IN} = 0.125 V rms, R_L = 100 Ω	±5	90	110		MHz
Bandwidth (0.1 dB)	G = +2, R_F = 499 Ω, V_{IN} = 0.125 V rms, R_L = 100 Ω	±15		10		MHz
Differential Slew Rate	V_{OUT} = 10 V p-p, G = +5, R_L = 100 Ω	±15	1400	1500		V/µs
Settling Time to 0.1%	10 V Step, G = +2	±15		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion (Differential)	f = 1 MHz, R_{LOAD} = 100 Ω, V_{OUT} = 40 V p-p	±15		–68		dBc
Input Voltage Noise	f = 10 kHz, G = +2 (Single Ended)	±5, ±15		1.85		nV/√Hz
Input Current Noise (+I_{IN})	f = 10 kHz, G = +2	±5, ±15		1.8		pA/√Hz
Input Current Noise (–I_{IN})	f = 10 kHz, G = +2	±5, ±15		19		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.05		%
Differential Phase Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.45		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5		5	12	mV
		±15		10	15	mV
	T_{MIN} to T_{MAX}				25	mV
Input Offset Voltage Drift				40		µV/°C
Differential Offset Voltage		±5, ±15		0.5	2	mV
	T_{MIN} to T_{MAX}				5	mV
Differential Offset Voltage Drift				5		µV/°C
–Input Bias Current		±5, ±15		20	60	µA
	T_{MIN} to T_{MAX}				100	µA
+Input Bias Current		±5, ±15		2	5	µA
	T_{MIN} to T_{MAX}				5	µA
Differential Input Bias Current		±5, ±15		10	50	µA
	T_{MIN} to T_{MAX}				50	µA
Open-Loop Transresistance	V_{OUT} = ±10 V, R_L = 100 Ω	±5, ±15	0.7	2		MΩ
	T_{MIN} to T_{MAX}		0.6			MΩ
INPUT CHARACTERISTICS						
Differential Input Resistance	+Input	±15		7		MΩ
	–Input			15		Ω
Differential Input Capacitance		±15		1.4		pF
Input Common-Mode Voltage Range		±15		13.5		±V
		±5		3.5		±V
Common-Mode Rejection Ratio	T_{MIN} to T_{MAX}	±5, ±15	56	60		dB
Differential Common-Mode Rejection Ratio	T_{MIN} to T_{MAX}	±5, ±15	80	100		dB
OUTPUT CHARACTERISTICS						
Voltage Swing	Single Ended, R_{LOAD} = 25 Ω	±15	23	24.5		V p-p
		±5	2.2	3.6		V p-p
	Differential, R_{LOAD} = 50 Ω	±15	46	49		V p-p
	T_{MIN} to T_{MAX}	±15	45			V p-p
Continuous Output Current	R_{LOAD} = 5 Ω	±15	500	750		mA
		±5	200	100		mA
Peak Output Current	10 µs Pulse, 1% Duty Cycle, R_L = 15 Ω	±15		1.0		A
Short Circuit Current	Note 1	±15		1.0		A

NOTES

[1]See Power Considerations section.

Specifications subject to change without notice.

RECEIVER AMPLIFIERS (@ T_A = +25°C, V_S = ±15 V dc, R_F = 1 kΩ and R_{LOAD} = 500 Ω unless otherwise noted)

Model	Conditions	V_S	AD816A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Small Signal Bandwidth (–3 dB)	G = +2, R_L = 100 Ω	±15		100		MHz
	G = +2, R_L = 100 Ω	±5		80		MHz
Bandwidth (0.1 dB)	G = +2	±15		30		MHz
	G = +2	±5		40		MHz
Slew Rate	V_{OUT} = 4 V p-p	±15		180		V/µs
Settling Time to 0.1%	V_{OUT} = 10 V p-p Step, G = +2	±15		45		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f = 1 MHz, R_{LOAD} = 200 Ω	±15		–68		dBc
Input Voltage Noise	f = 10 kHz	±5, ±15		4		nV/√Hz
Current Noise	f = 10 kHz	±5, ±15		2		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_{LOAD} = 150 Ω	±15		0.04	0.08	%
		±5		0.05	0.1	%
Differential Phase Error	NTSC, G = +2, R_{LOAD} = 150 Ω	±15		0.03	0.1	Degrees
		±5		0.06	0.1	Degrees
DC PERFORMANCE						
Input Offset Voltage		±5, ±15		7.5	15	mV
	T_{MIN} to T_{MAX}				15	mV
Offset Voltage Drift				20		µV/°C
Input Bias Current		±5, ±15		5	7	µA
	T_{MIN} to T_{MAX}				15	µA
Input Offset Current		±5, ±15		0.5	2	µA
Offset Current Drift				1		nA/°C
Open-Loop Gain	V_{OUT} = ±7.5 V, R_{LOAD} = 150 Ω	±15	3	6		V/mV
	T_{MIN} to T_{MAX}	±15	1			V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±15	+13	+14.3		V
		±15	–12	–13.4		V
		±5	+3.8	+4.3		V
		±5	–2.7	–3.4		V
Common-Mode Rejection Ratio	V_{CM} = ±5 V	±15	82	110		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	Single Ended, R_{LOAD} = 150 Ω	±15	25.2	25.5		V p-p
	T_{MIN} to T_{MAX}	±15	25.2			V p-p
	Single Ended, R_{LOAD} = 150 Ω	±5	6.2	6.4		V p-p
	T_{MIN} to T_{MAX}	±5	6.0			V p-p
Output Current	R_L = 150 Ω	±15	65	70		mA
Short Circuit Current		±15		105		mA

Specifications subject to change without notice.

COMMON CHARACTERISTICS (@ T_A = +25°C, V_S = ±15 V dc, R_F = 1 kΩ and R_{LOAD} = 50 Ω (Driver), R_{LOAD} = 500 Ω (Receiver) unless otherwise noted)

	Conditions	V_S	AD816A Min	Typ	Max	Units
MATCHING CHARACTERISTICS						
Crosstalk:						
Driver to Driver	f = 1 MHz, V_{IN} = 200 mV rms, R_{LOAD} = 100 Ω	±15		–67		dB
Drivers to Receivers	f = 1 MHz, V_{IN} = 200 mV rms, R_{LOAD} = 100 Ω	±15		–64		dB
Receiver to Receiver	f = 1 MHz, V_{IN} = 200 mV rms, R_{LOAD} = 500 Ω	±15		–81		dB
POWER SUPPLY						
Operating Range			±5		±18	V
Quiescent Current		±15		46	56	mA
	T_{MIN} to T_{MAX}	±15			59	mA
Driver Supply Rejection Ratio	T_{MIN} to T_{MAX}	±15, ±5	–49	–66		dB
Receiver Supply Rejection Ratio	T_{MIN} to T_{MAX}	±15, ±5	–69	–75		dB

Specifications subject to change without notice.

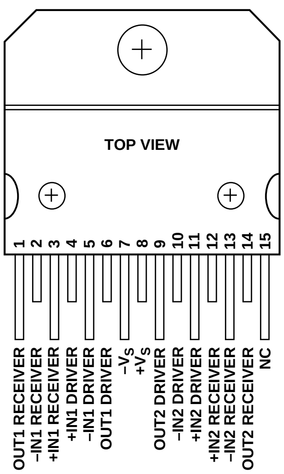
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V Total
Internal Power Dissipation[2]
  Plastic (Y, YS & VR) . 3.05 Watts (Observe Derating Curves)
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±6 V
Output Short Circuit Duration
  . . . . Observe Power Derating Curves
Storage Temperature Range
  Y, YS, VR Package . . . . –65°C to +125°C
Operating Temperature Range
  AD816A . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 10 sec) . . . . +300°C

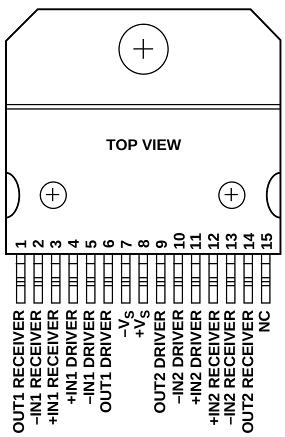
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 15-Pin Through Hole and Surface Mount: θ_{JA} = 41°C/Watt.

PIN CONFIGURATION

Y-15



VR-15, YS-15



MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD816 is limited by the associated rise in junction temperature. The maximum safe junction temperature for the plastic encapsulated parts is determined by the glass transition temperature of the plastic, about 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

The AD816 has thermal shutdown protection, which guarantees that the maximum junction temperature of the die remains below a safe level. However, shorting the output to ground or either power supply for an indeterminate period will result in device failure. To ensure proper operation, it is important to observe the derating curves and refer to the section on power considerations.

It must also be noted that in high (noninverting) gain configurations (with low values of gain resistor), a high level of input overdrive can result in a large input error current, which may result in a significant power dissipation in the input stage. This power must be included when computing the junction temperature rise due to total internal power.

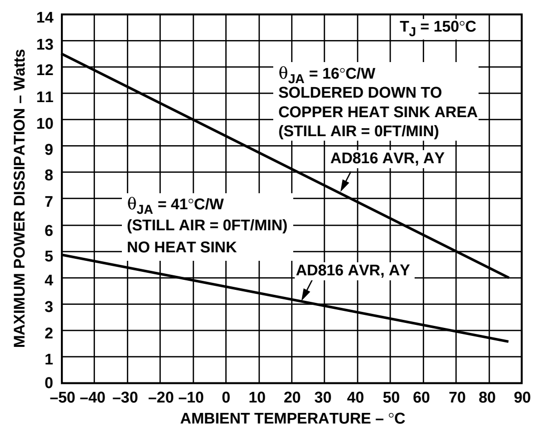


Figure 1. Plot of Maximum Power Dissipation vs. Temperature (Copper Heat Sink Area = 2 in.²)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD816AY	–40°C to +85°C	15-Pin Through-Hole SIP with Staggered Leads & 90° Lead Form	Y-15
AD816AYS	–40°C to +85°C	15-Pin Through-Hole SIP with Staggered Leads & Straight Lead Form	YS-15
AD816AVR	–40°C to +85°C	15-Pin Surface Mount DDPAK	VR-15

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD816 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



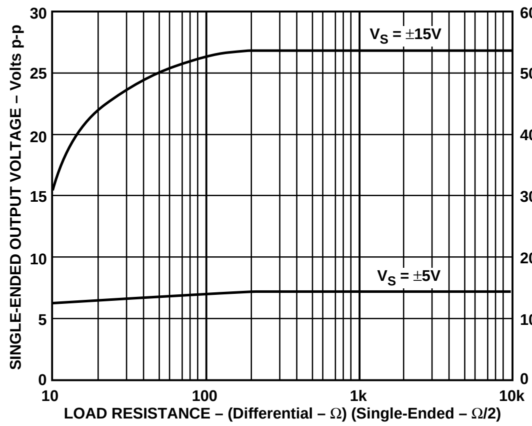


Figure 2. Driver Output Voltage Swing vs. Load Resistance

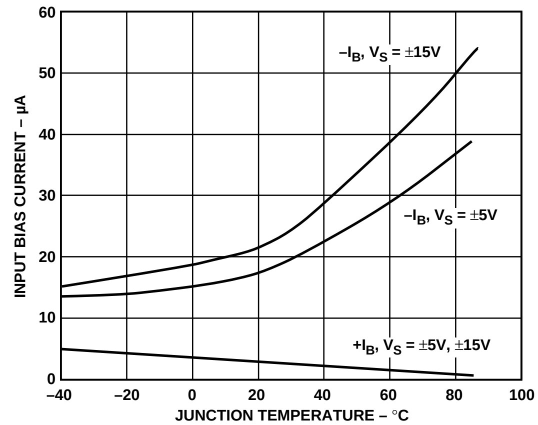


Figure 5. Driver Input Bias Current vs. Temperature

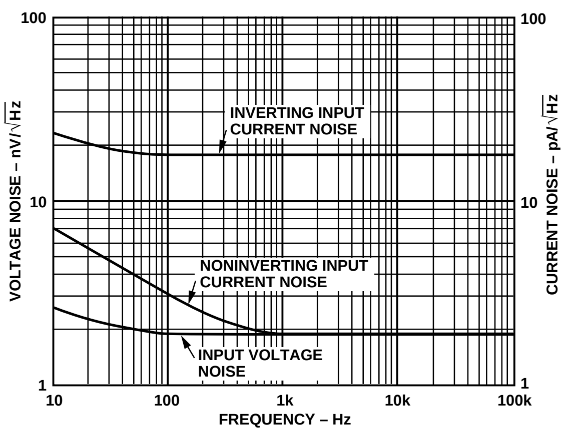


Figure 3. Driver Input Current and Voltage Noise vs. Frequency

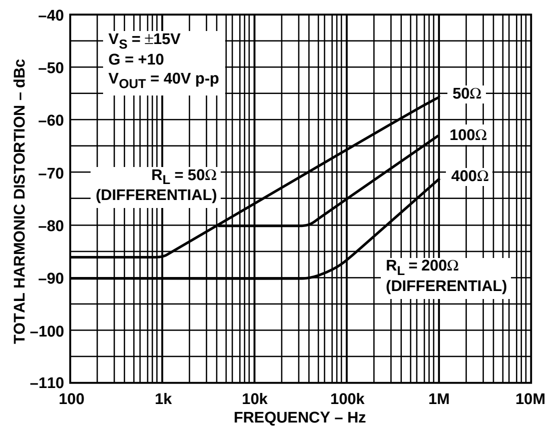


Figure 6. Driver Total Harmonic Distortion vs. Frequency

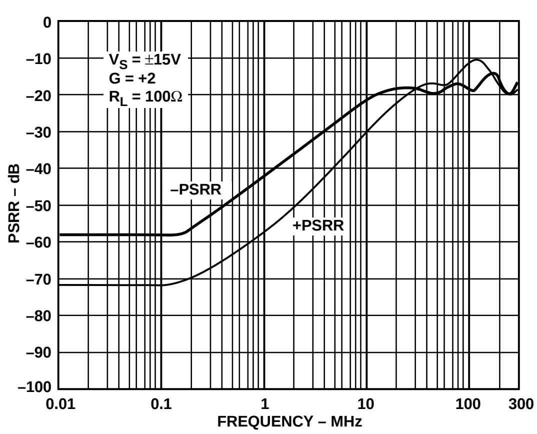


Figure 4. Driver Power Supply Rejection vs. Frequency

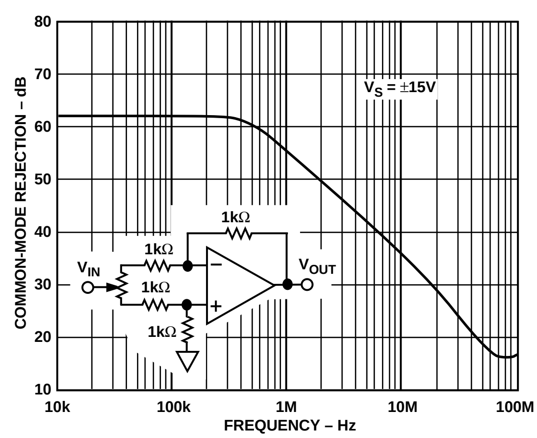


Figure 7. Driver Common-Mode Rejection vs. Frequency

AD816–Typical Driver Performance Characteristics

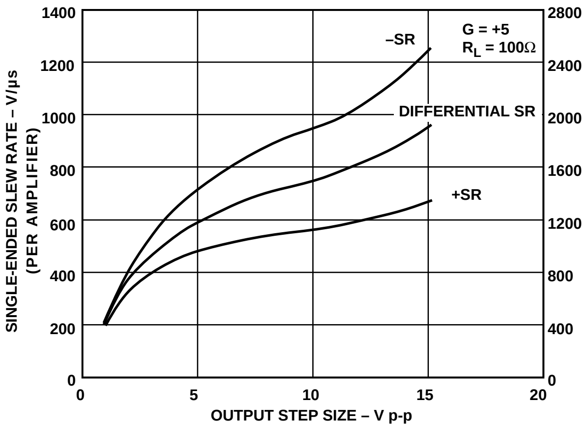


Figure 8. Driver Slew Rate vs. Output Step Size

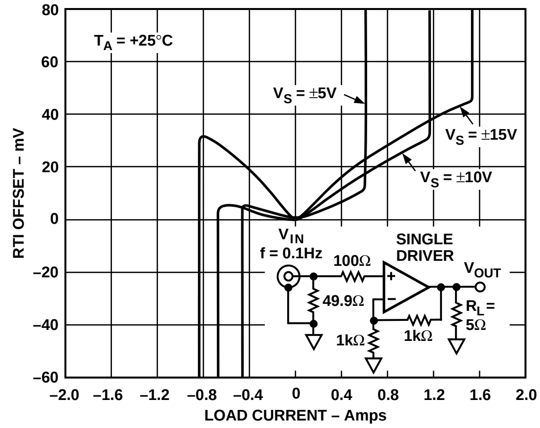


Figure 11. Driver Thermal Nonlinearity vs. Output Current Drive

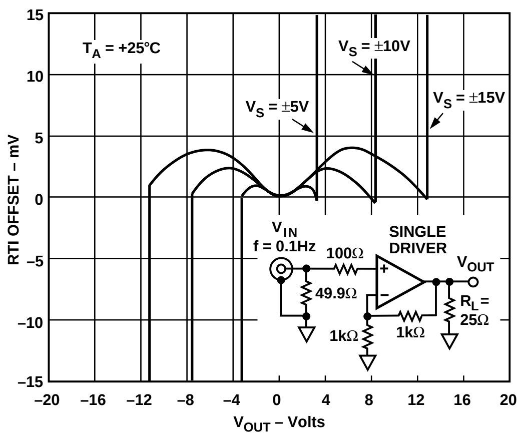


Figure 9. Driver Gain Nonlinearity vs. Output Voltage

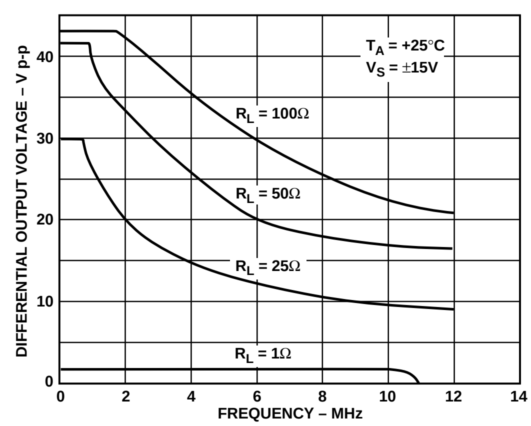


Figure 12. Driver Large Signal Frequency Response

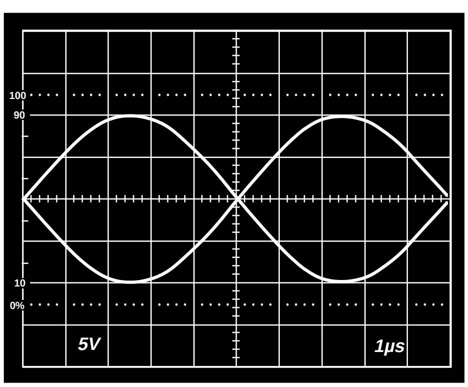


Figure 10. Driver 40 V p-p Differential Sine Wave; R_L = 50 Ω, f = 100 kHz

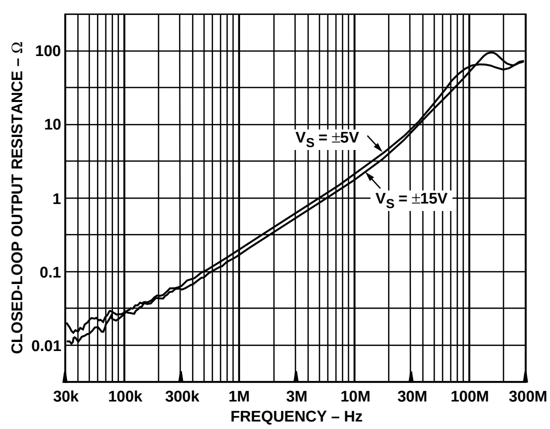


Figure 13. Driver Closed-Loop Output Resistance vs. Frequency

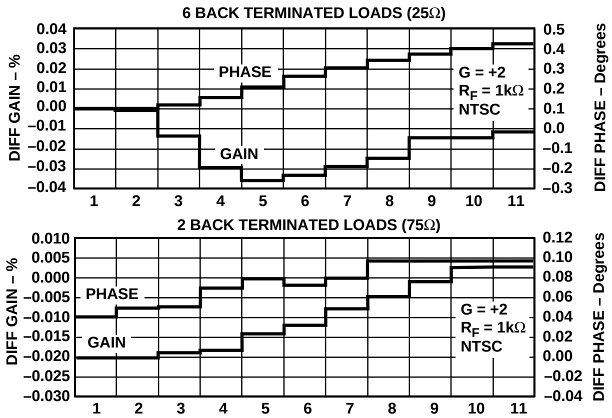


Figure 14. Driver Differential Gain and Differential Phase (Per Amplifier)

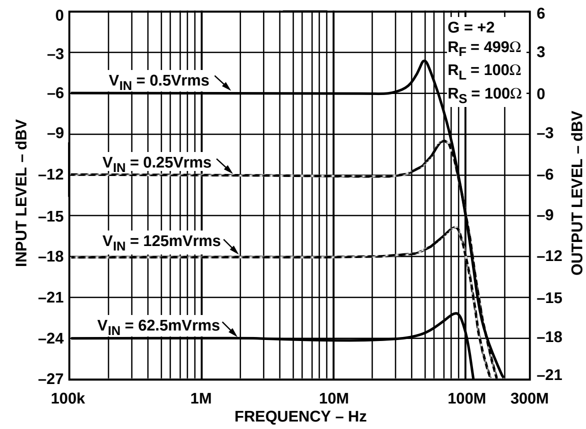


Figure 17. Driver Small and Large Signal Frequency Response, G = +2

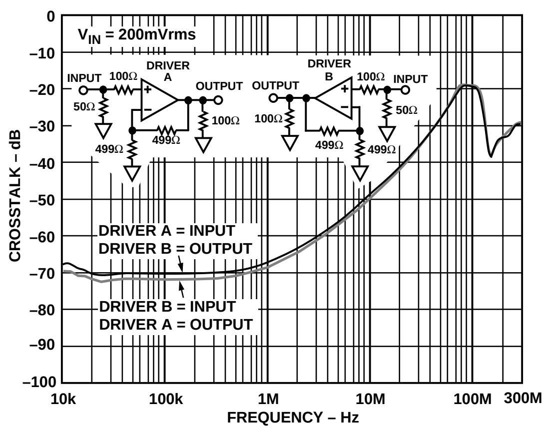


Figure 15. Driver Output-to-Output Crosstalk vs. Frequency

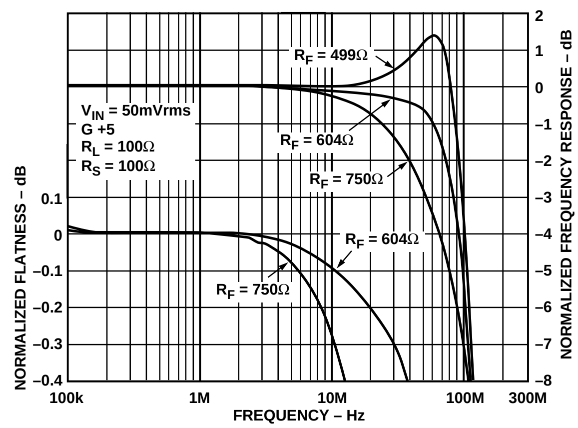


Figure 18. Driver Frequency Response and Flatness, G = +5

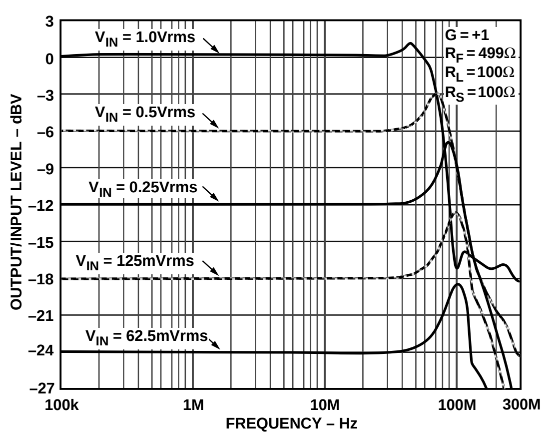


Figure 16. Driver Small and Large Signal Frequency Response, G = +1

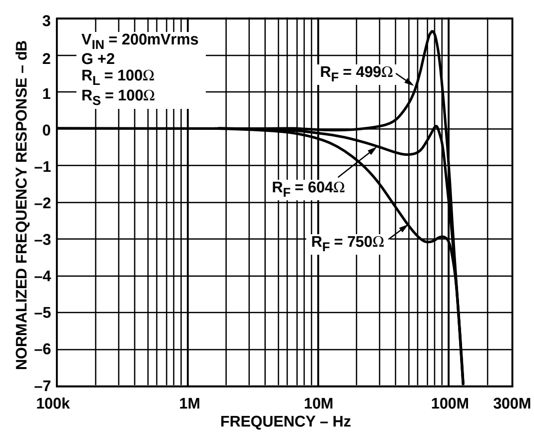


Figure 19. Driver Frequency Response vs. R_F, G = +2

AD816–Typical Driver Performance Characteristics

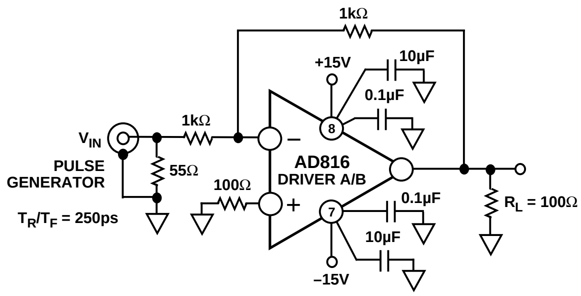


Figure 20. Test Circuit Gain = –1

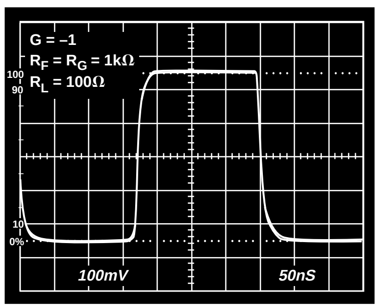


Figure 21. Driver 500 mV Step Response, G = –1

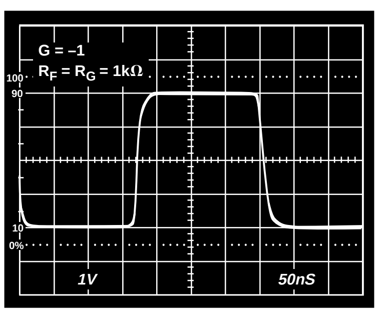


Figure 22. Driver 4 V Step Response, G = –1

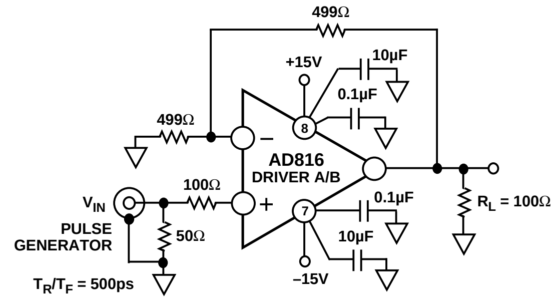


Figure 23. Driver Test Circuit, Gain = +2

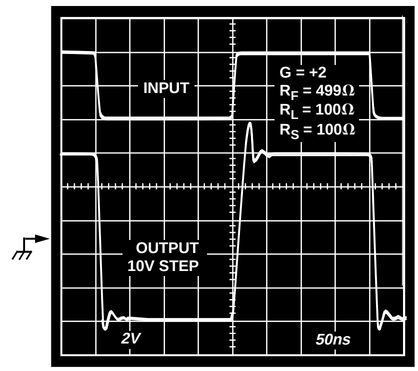


Figure 24. 10 V Step Response, G = +2

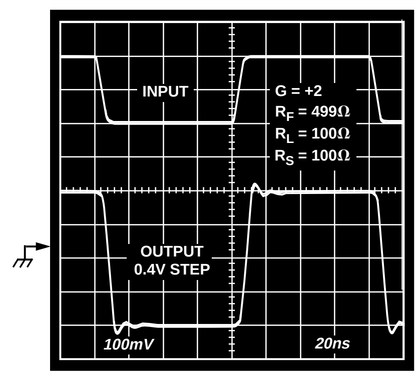


Figure 25. Driver 400 mV Step Response, G = +2

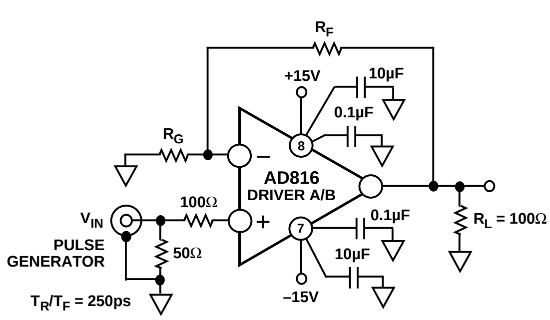


Figure 26. Test Circuit, Gain = 1 + R_F/R_G

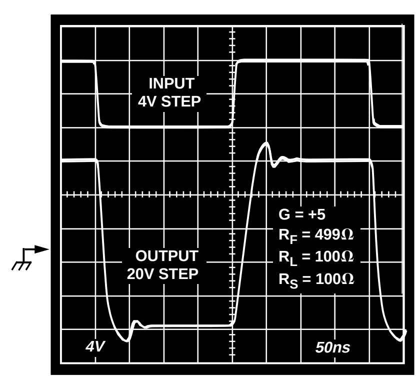


Figure 27. Driver 20 V Step Response, G = +5

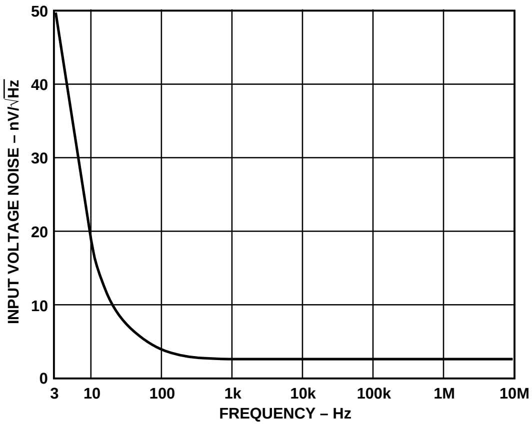


Figure 28. Receiver Input Voltage Noise Spectral Density

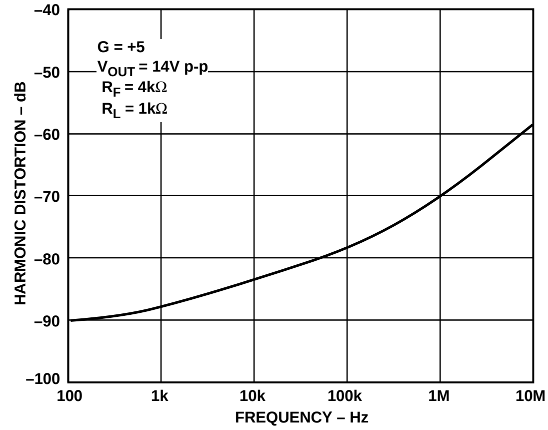


Figure 31. Receiver Harmonic Distortion vs. Frequency

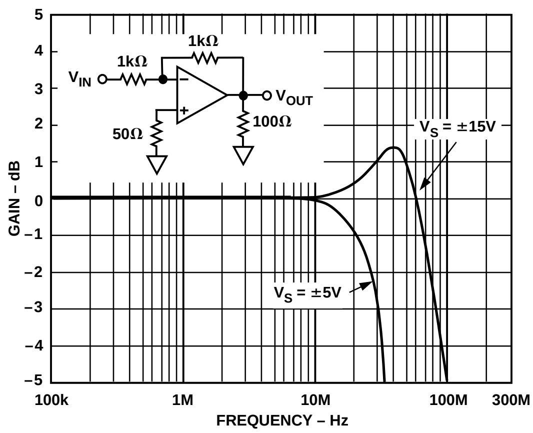


Figure 29. Receiver Closed-Loop Gain vs. Frequency, Gain = –1

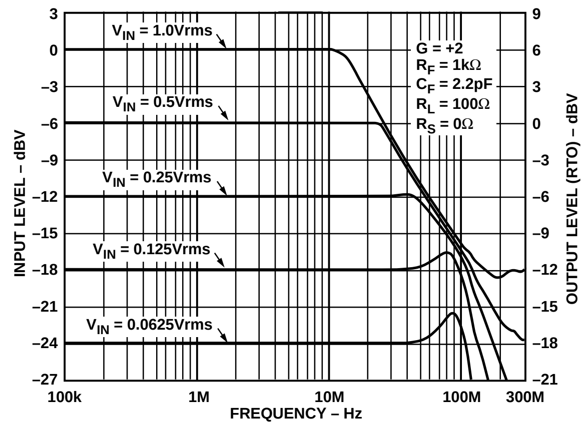


Figure 32. Receiver Small and Large Signal Frequency Response, Gain = +2

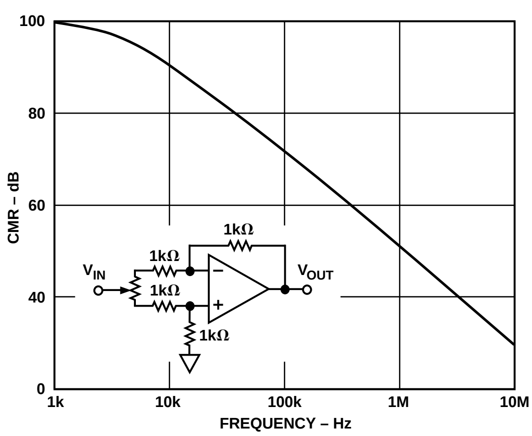


Figure 30. Receiver Common-Mode Rejection vs. Frequency

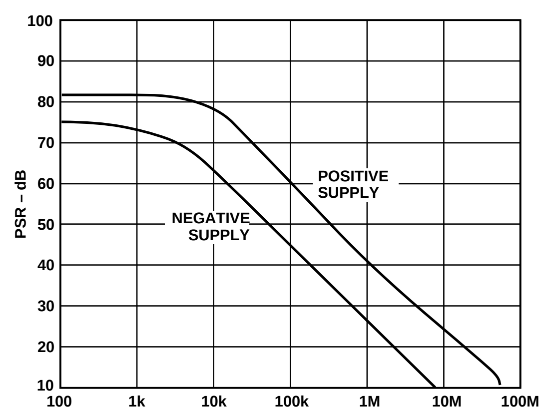


Figure 33. Receiver Power Supply Rejection vs. Frequency

AD816–Typical Receiver Performance Characteristics

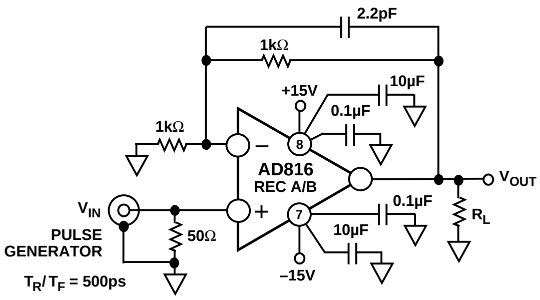


Figure 34. Test Circuit, Gain = +2

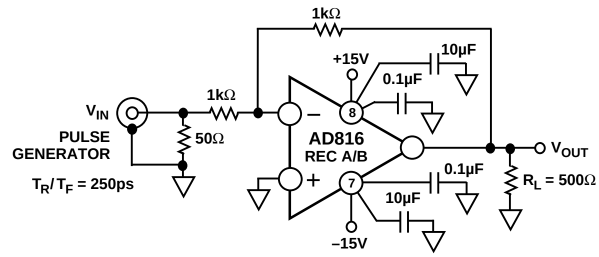


Figure 37. Test Circuit, Gain = −1

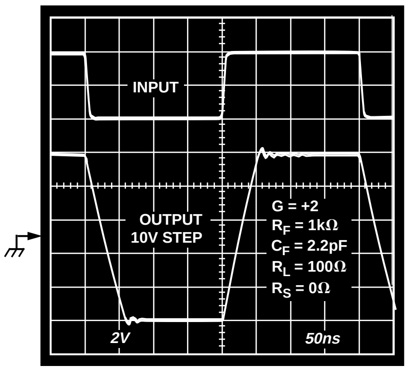


Figure 35. Receiver 10 V Step Response, G = +2

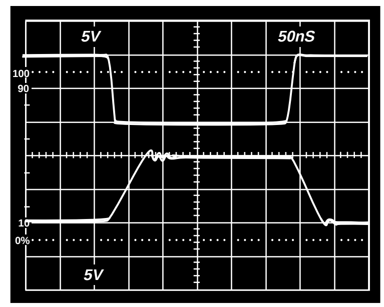


Figure 38. Receiver 10 V Step Response, G = −1

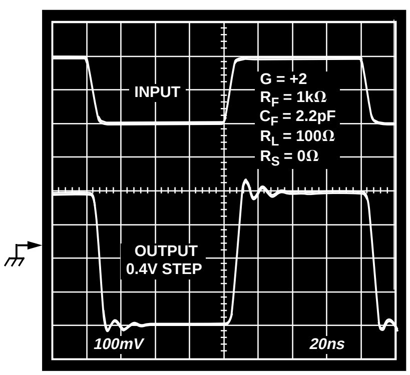


Figure 36. Receiver 400 mV Step Response, G = +2

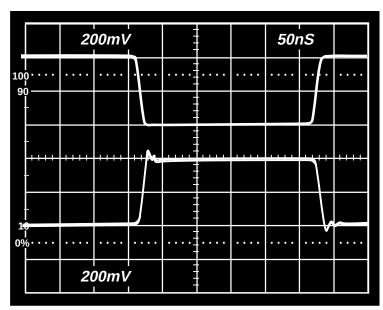


Figure 39. Receiver 400 mV Step Response, G = −1

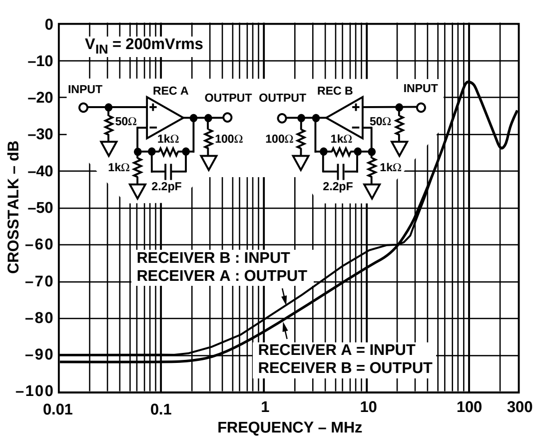


Figure 40. Receiver Output-to-Output Crosstalk vs.Frequency

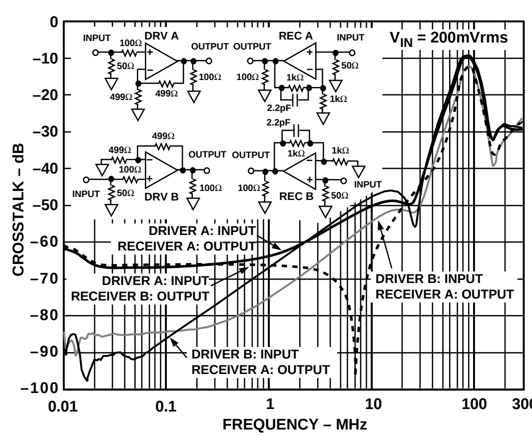


Figure 41. Driver-to-Receiver Crosstalk vs. Frequency

THEORY OF OPERATION (DRIVER)

The AD816 driver is a dual current feedback amplifier with high (500 mA) output current capability. Being a current feedback amplifier, the AD816 driver's open-loop behavior is expressed as transimpedance, $\Delta V_O/\Delta I_{-IN}$, or T_Z. The open-loop transimpedance behaves just as the open-loop voltage gain of a voltage feedback amplifier, that is, it has a large dc value and decreases at roughly 6 dB/octave in frequency.

Since R_{IN} is proportional to $1/g_M$, the equivalent voltage gain is just $T_Z \times g_M$, where the g_M in question is the transconductance of the input stage. Figure 42 shows the driver connected as a follower with gain. Basic analysis yields the following results:

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$R_{IN} = 1/g_M \approx 25\ \Omega$

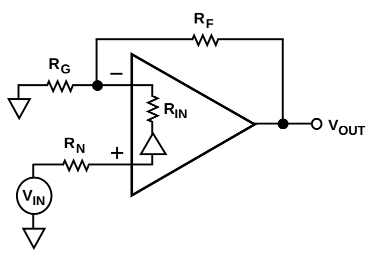


Figure 42. Current-Feedback Amplifier Operation

Recognizing that $G \times R_{IN} << R_F$ for low gains, it can be seen to the first order that bandwidth for this amplifier is independent of gain (G).

Considering that additional poles contribute excess phase at high frequencies, there is a minimum feedback resistance below which peaking or oscillation may result. This fact is used to determine the optimum feedback resistance, R_F. In practice parasitic capacitance at the inverting input terminal will also add phase in the feedback loop so that picking an optimum value for R_F can be difficult.

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

Choice of Feedback and Gain Resistors

The fine scale gain flatness will, to some extent, vary with feedback resistance. It is therefore recommended that once optimum resistor values have been determined, 1% tolerance values should be used if it is desired to maintain flatness over a wide range of production lots. Table I shows optimum values for several useful gain configurations. These should be used as a starting point in any application.

Table I. Driver Resistor Values

	R_F (Ω)	R_G (Ω)
G = +1	604	∞
–1	499	499
+2	499	499
+5	499	125
+10	1k	110

DRIVER DC ERRORS AND NOISE

There are three major noise and offset terms to consider in a current feedback amplifier. For offset errors refer to the equation below. For noise error the terms are root-sum-squared to give a net output error. In the circuit below (Figure 43), they are input offset (V_{IO}) which appears at the output multiplied by the noise gain of the circuit ($1 + R_F/R_G$), noninverting input current ($I_{BN} \times R_N$) also multiplied by the noise gain, and the inverting input current, which when divided between R_F and R_G and subsequently multiplied by the noise gain always appear at the output as $I_{BI} \times R_F$. The input voltage noise of the AD816 is less than 4 nV/√Hz. At low gains, however, the inverting input current noise times R_F is the dominant noise source. Careful layout and device matching contribute to better offset and drift. The typical performance curves in conjunction with the equations below can be used to predict the performance of the AD816 in any application.

$$V_{OUT} = VIO\left(1 + \frac{R_F}{R_G}\right) \pm I_{BN}\ R_N \left(1 + \frac{R_F}{R_G}\right) \pm I_{BI}\ R_F$$

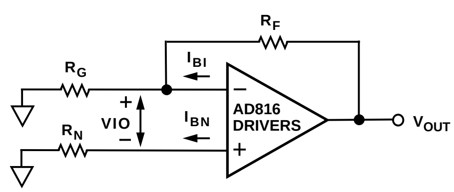


Figure 43. Driver Output Offset Voltage

THEORY OF OPERATION (RECEIVER)

Each AD816 receiver is a wide band high performance operational amplifier. It also provides a constant slew rate, bandwidth and settling time over its entire specified temperature range.

The AD816 receiver consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which deliver the necessary current to the load while maintaining low levels of distortion.

A protection resistor in series with the noninverting input is required in circuits where the input to the receiver could be subject to transients on continuous overload voltages exceeding the ±6 V maximum differential limit. The resistor provides protection for the input transistors, by limiting their maximum base current.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed-loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (5 mm min) should be left around the signal lines to minimize coupling.

POWER SUPPLY BYPASSING

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 µF) will be required to provide the best settling time and lowest distortion. A parallel combination of 10.0 µF and 0.1 µF is recommended. Under some low frequency applications, a bypass capacitance of greater than 10 µF may be necessary. Due to the large load currents delivered by the AD816, special consideration must be given to careful bypassing. The ground returns on both supply bypass capacitors as well as signal common must be "star" connected as shown in Figure 44.

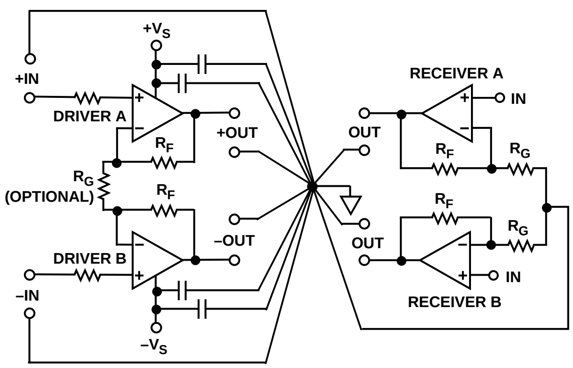


Figure 44. Signal Ground Connected in "Star" Configuration

POWER CONSIDERATIONS

The 500 mA drive capability of the AD816 driver enables it to drive a 50 Ω load at 40 V p-p when it is configured as a differential driver. This implies a power dissipation, P_{IN}, of nearly 5 watts. To ensure reliability, the junction temperature of the AD816 should be maintained at less than 175°C. For this reason, the AD816 will require some form of heat sinking in most applications. The thermal diagram of Figure 45 gives the basic relationship between junction temperature (T_J) and various components of θ_{JA}.

$$T_J = T_A + P_{IN}\ \theta_{JA} \qquad \text{Equation 1}$$

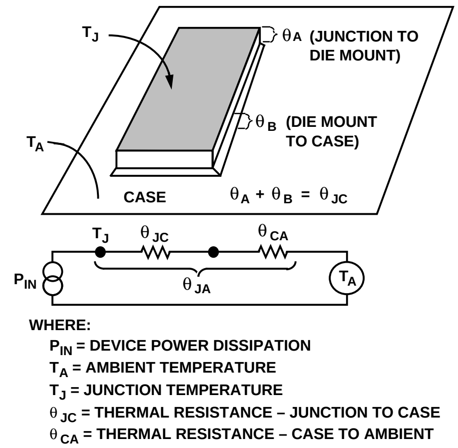


Figure 45. A Breakdown of Various Package Thermal Resistances

Figure 46 gives the relationship between output voltage swing into various loads and the power dissipated by the AD816 (P_{IN}). This data is given for both sine wave and square wave (worst case) conditions. It should be noted that these graphs are for mostly resistive (phase < ±10°) loads. When the power dissipation requirements are known, Equation 1 and the graph on Figure 47 can be used to choose an appropriate heat sinking configuration.

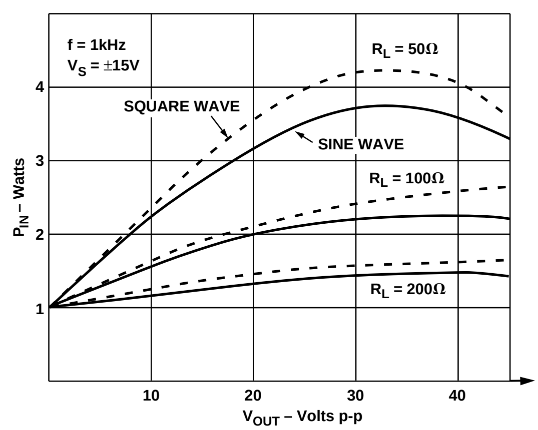


Figure 46. Total Power Dissipation vs Differential Driver Output Voltage

Normally, the AD816 will be soldered directly to a copper pad. Figure 47 plots θ_{JA} against size of copper pad. This data pertains to copper pads on both sides of G10 epoxy glass board connected together with a grid of feedthroughs on 5 mm centers.

This data shows that loads of 100 ohms or greater will usually not require any more than this. This is a feature of the AD816's 15-lead power SIP package.

An important component of θ_{JA} is the thermal resistance of the package to heatsink. The data given is for a direct soldered connection of package to copper pad. The use of heatsink grease either with or without an insulating washer will increase this number. Several options now exist for dry thermal connections. These are available from Bergquist as part # SP600-90. Consult with the manufacturer of these products for details of their application.

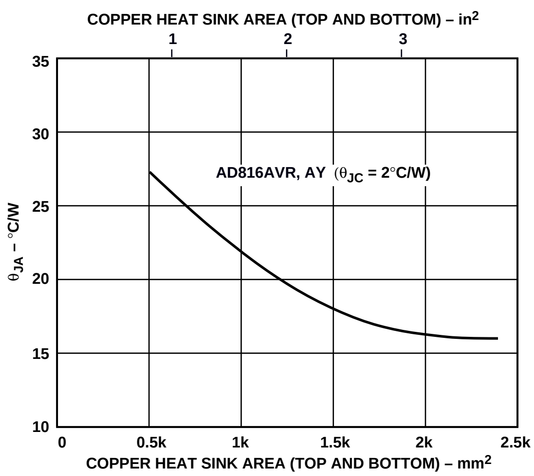


Figure 47. Power Package Thermal Resistance vs. Heat Sink Area

Other Power Considerations

There are additional power considerations applicable to the AD816. First, as with many current feedback amplifiers, there is an increase in supply current when delivering a large peak-to-peak voltage to a resistive load at high frequencies. This behavior is affected by the load present at the amplifier's output. Figure 12 summarizes the full power response capabilities of the AD816 driver. These curves apply to the differential driver applications (right-hand side of Figure 52). In Figure 12, maximum continuous peak-to-peak output voltage is plotted vs. frequency for various resistive loads. Exceeding this value on a continuous basis can damage the AD816.

The AD816 is equipped with a thermal shutdown circuit. This circuit ensures that the temperature of the AD816 die remains below a safe level. In normal operation, the circuit shuts down the AD816 at approximately 180°C and allows the circuit to turn back on at approximately 140°C. This built-in hysteresis means that a sustained thermal overload will cycle between power-on and power-off conditions. The thermal cycling typically occurs at a rate of 1 ms to several seconds, depending on the power dissipation and the thermal time constants of the package and heat sinking. Figures 48 and 49 illustrate the thermal shutdown operation after driving OUT1 to the + rail, and OUT2 to the – rail, and then short-circuiting to ground each output of the AD816. The AD816 will not be damaged by momentary operation in this state, but the overload condition should be removed.

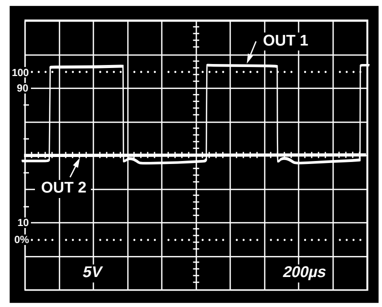


Figure 48. OUT2 Shorted to Ground Through a 2 Ω Resistor, Square Wave Is OUT1, R_F = 1 kΩ, R_G = 222 Ω

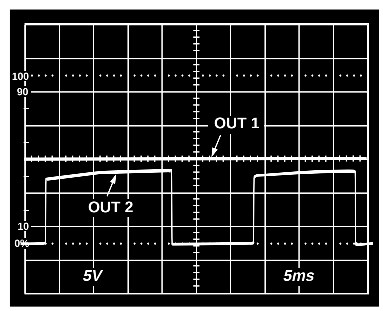


Figure 49. OUT1 Shorted to Ground Through a 2 Ω Resistor, Square Wave Is OUT2, R_F = 1 kΩ, R_G = 222 Ω

APPLICATIONS

ADSL Transceiver

The AD816 is designed for the primary purpose of providing an integrated solution for the transmit and receive functions of an ADSL modem. ADSL or Asymmetrical Digital Subscriber Line is a means for delivering up to 6 Mbps from a telephone central office (CO) into a home over the conventional telephone twisted pair (local loop) and a few hundred kbps simultaneously in the opposite direction.

The transmit/receive block is commonly referred to as a hybrid, which is an old telephone term, and the function was originally performed with passive circuitry in early phone systems. The hybrid's function is to deliver maximum transmit power down the line, while providing the receive circuitry with a maximum receive signal and a minimized (self) transmit signal. As the line gets longer, this separation becomes much more difficult, because the transmit signal must be larger to reach the other end with acceptable SNR, while the receive signal is more attenuated by the longer line.

The figure of merit for the performance of the hybrid is commonly called trans-hybrid loss and is a measure of how much the transmit signal that appears in the receive circuit has been attenuated relative to the amplitude of the transmit signal itself. It is measured in dBs and is a function of frequency.

In addition to the passive circuits that have been used over time, active circuit techniques can enhance the hybrid's performance. Figure 50 shows one of the various hybrid circuits that uses the AD816 in an ADSL application. The high power op amps serve as the transmitter, while the low noise amplifiers serve as the receiver.

The power amplifiers of the AD816 (D1 and D2) are arranged in a differential configuration that receives its inputs from the differential outputs of a D/A converter. The outputs differentially drive the transformer primary with a turns ratio of 1:2. The line on the secondary side of the transformer has an impedance of 120 Ω. Thus one quarter of this resistance (30 Ω) is required for back termination on the primary side due to the impedance scaling by the square of the turns ratio. This resistance is divided in half (15 Ω) and put on each side of the drive buffers for symmetry (R101 and R201).

The receive section (R1 and R2) is configured as a pair of difference amplifiers that together produce a differential output that consists of the receive signal in addition to the transmit signal attenuated by the trans-hybrid loss.

The circuit is highly symmetrical, so a single-ended explanation can be easily generalized to understand the differential operation. D1 output terminals (Pin 6 of the AD816) drives the top of the primary of T1 through R101. A voltage divider is formed

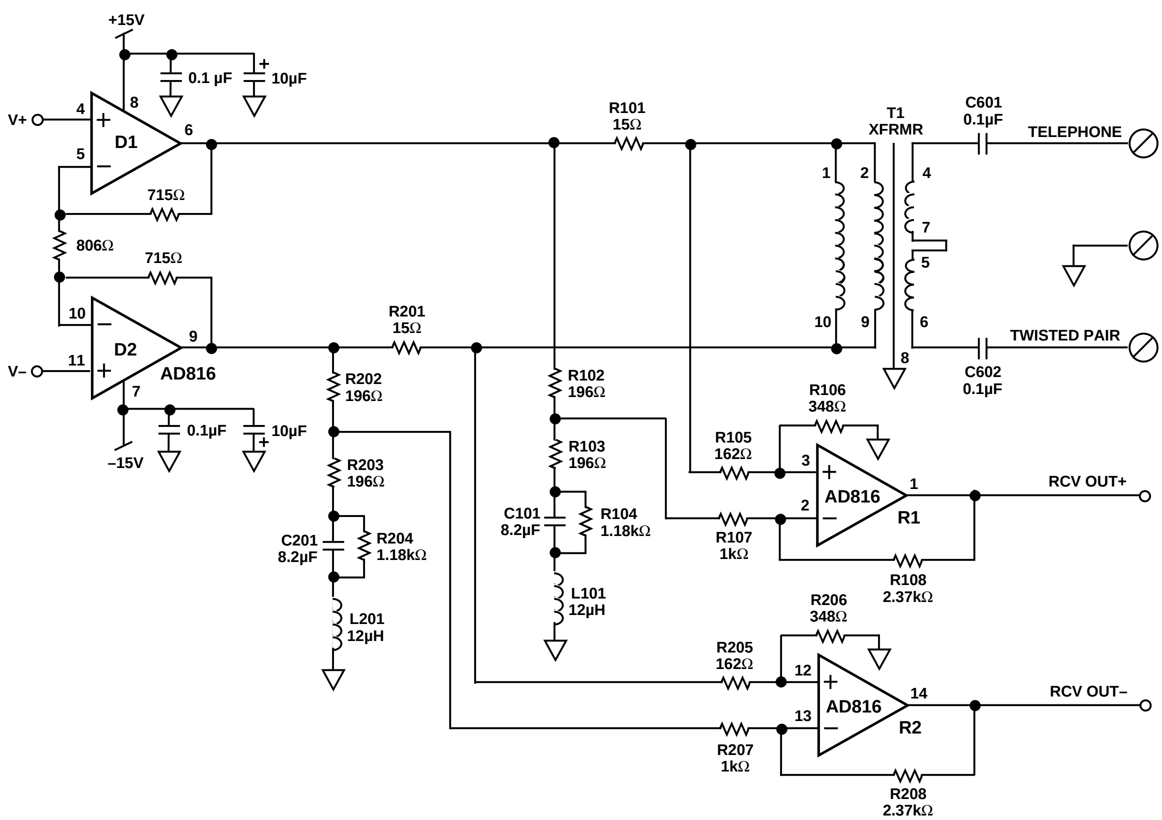


Figure 50. AD816 as an ADSL Transceiver

by R101 and all the downstream circuitry comprised of T1, the transmission line and its termination. For an ideal transformer, transmission line and termination, this will appear to be 15 Ω, and thus the signal appearing at Pins 1 and 2 of T1 will be the output of D1 divided by two in the ideal case. This signal is applied to the input of R1 (Receive 1 of the AD816) (Pin 3) via R105.

In some ADSL systems (DMT), there is a need to transmit higher crest factor signals. Typically this is done by increasing the turns ratio of T1 to as much as 4:1. In this case, R101 and R201 would be 3.75 Ω, and the peak current of the AD816 (1 A) would be the drive limit of the transmitter.

R1 is configured as a difference amplifier. The negative side (Pin 2) is driven by another signal that is a divided down version of the output of D1. This circuit is formed by R102 as one side of the voltage divider along with R103, C101, R104 and L101 as the other half of the divider. If the frequency dependent impedance part of this circuit matches the transformer, transmission line and termination impedance, then the signals applied to both sides of the difference-amp-configured R1 will be the same, and the transmit signal will be totally subtracted out by the circuit.

In a real-world situation, it is not practical (or even possible) to subtract out all of the transmit signal (100% trans-hybrid loss), but only provide a first order cancellation which goes a long way toward reducing the dynamic range of the RCVOUT signal. The overall performance of this circuit depends on the ability to build a lumped element network that matches the impedance of the transmission line over the frequency range required for ADSL (≈ 20 kHz to 1.1 MHz).

The circuits formed by D2 and R2 of the AD816 are totally symmetric with those formed by D1 and R1 and work in the same fashion. All the components in the D1, R1 circuits that are numbered with 100 range numbers are numbered with 200 range numbers in the D2, R2 circuits.

The receive signal from the telephone line creates a differential signal across the primary of T1. There is, however, a two to one reduction in amplitude due to turns ratio of T1. This differential signal is applied to the + inputs (Pins 3 and 12) of R1 and R2. The receive amplifiers buffer this signal and present a differential output at Pins 1 and 14. There is no significant receive signal applied to the negative inputs of R1 and R2 due to the attenuating effects of R101 and R201 and the low output impedances of D1 and D2.

Thus, the overall circuit provides first order cancellation of the transmit signal and differential buffering of the receive signal.

Dual Composite Amplifier

A composite amplifier uses two different op amps together in a circuit to yield an overall performance that has some of the advantages of each op amp. In the case of the AD816, two composite amplifiers can be constructed that offer the low noise of the receiver amps in addition to the high current output of the driver amps.

The circuit in Figure 51 shows an example of such a circuit. It uses receiver amp R1 for the low noise first stage and driver D1 for the high output current second stage. Both local and overall feedback are used to get the desired response.

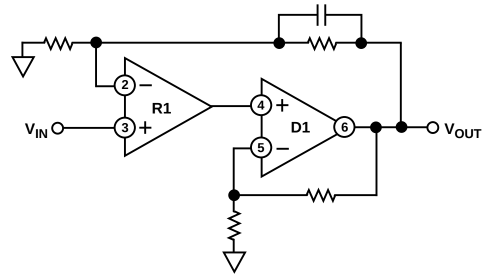


Figure 51. AD816 Composite Amplifier

Creating Differential Signals

If only a single-ended signal is available to drive the AD816 and a differential output signal is desired, a circuit can be used to perform the single-ended to differential conversion.

The circuit shown in Figure 52 performs this function. It uses the AD816 with the gain of one receiver set at +1 and the gain of the other at –1. The 1 kΩ resistor across the input terminals of the follower makes the noise gain (NG = 2) equal to the inverter's. The two receiver outputs then differentially drive the inputs to the AD816 driver with no common-mode signal to first order.

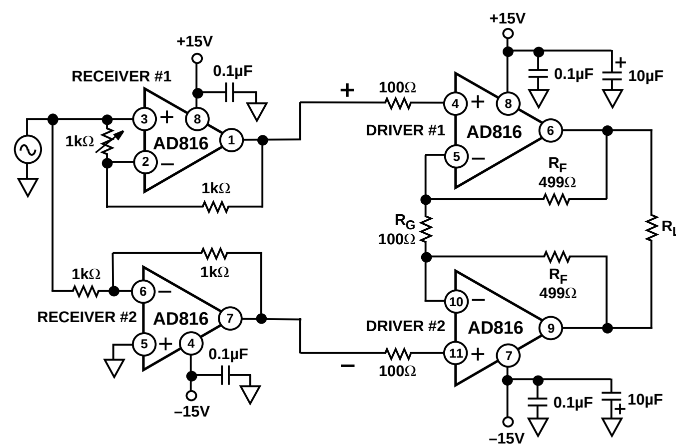
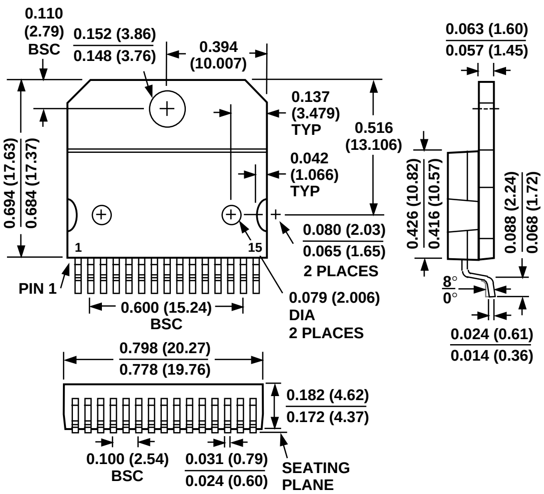


Figure 52. Differential Driver with Single-Ended Differential Converter

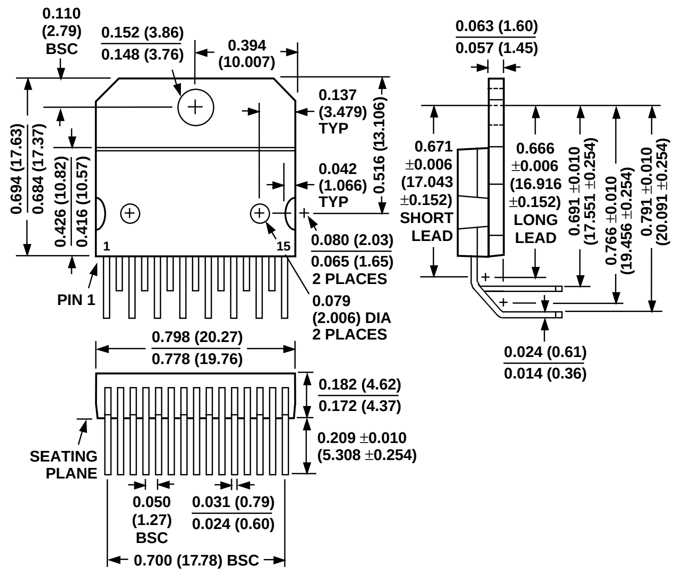
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

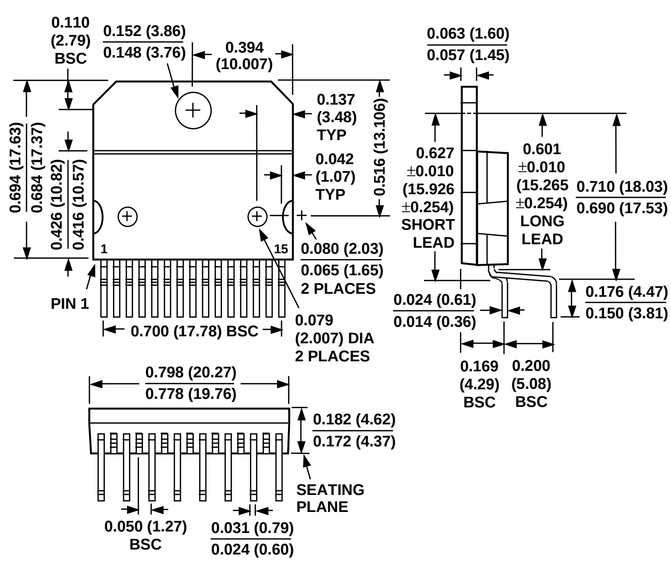
15-Pin Surface Mount DDPAK (VR-15)



15-Pin Through Hole SIP with Staggered Leads and 90° Lead Form (Y-15)



15-Pin Through Hole SIP with Staggered Leads and Straight Lead Form (YS-15)



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